Halo Implant in Semiconductor Structures

DESCRIPTION

[Para 1] Background of the Invention

[Para 2] 1. Technical Field

[Para 3] The present invention relates to performance improvements of semiconductor transistors, and more particularly, to the use of halo implants to improve performance of semiconductor transistors.

[Para 4] 2. Related Art

[Para 5] In the fabrication process of a typical semiconductor transistor, halo implant is a fabrication step which involves the doping of regions beneath the lightly-doped source/drain (S/D) extension regions of the transistor so as to form halo regions. For each of such halo regions, only the portion under the gate region (called undercutting portion) is useful, and therefore desirable, whereas the rest of the halo region has the effect of reducing the doping concentration of the respective S/D region (called the S/D doping reduction effect), which is undesirable.

[Para 6] Therefore, there is a need for a novel method for forming a halo region that minimizes the S/D doping reduction effect.

[Para 7] Summary of the Invention

[Para 8] The present invention provides a halo implant method, comprising the steps of (a) providing first and second semiconductor structures formed on a same semiconductor substrate, wherein the first semiconductor structure comprises a first gate region, a first channel region, and first and second semiconductor regions, wherein the first gate region is on top of the first

channel region and is oriented in a first direction, wherein the first channel region is sandwiched between the first and second semiconductor regions, wherein the second semiconductor structure comprises a second gate region, a second channel region, and third and fourth semiconductor regions, wherein the second gate region is on top of the second channel region and is oriented in a second direction, wherein the second channel region is sandwiched between the third and fourth semiconductor regions, and wherein the first and second channel regions are of a same channel polarity, wherein the first and second directions are essentially parallel to a top surface of the semiconductor substrate and are not parallel to each other; and (b) halo-implanting the first, second, third, and fourth semiconductor regions in a third projected direction, wherein the third projected direction is essentially a bisector direction of the first and second directions.

[Para 9] The present invention also provides a halo implant method, comprising the steps of (a) providing first and second semiconductor structures formed on a same semiconductor substrate, wherein the first semiconductor structure comprises a first gate region, a first channel region, and first and second semiconductor regions, wherein the first gate region is on top of the first channel region and is oriented in a first direction, wherein the first channel region is sandwiched between the first and second semiconductor regions, wherein the second semiconductor structure comprises a second gate region, a second channel region, and third and fourth semiconductor regions, wherein the second gate region is on top of the second channel region and is oriented in a second direction, wherein the second channel region is sandwiched between the third and fourth semiconductor regions, wherein the first and second channel regions are of a same channel polarity, wherein the first and second directions are essentially parallel to a top surface of the semiconductor substrate; and (b) if the first and second directions are not essentially parallel to each other, halo-implanting the first semiconductor region, but not the third and fourth semiconductor regions, in a third projected direction, wherein the third projected direction is essentially perpendicular to the first direction and going from the first semiconductor

region toward the first gate region; and (c) if the first and second directions are essentially parallel to each other, halo-implanting the first and third semiconductor regions, but not the second and fourth semiconductor regions, in a fourth projected direction, wherein the fourth projected direction is essentially perpendicular to the first direction and going from the first semiconductor region toward the first gate region.

[Para 10] The present invention also provides a semiconductor structure, comprising (a) first and second semiconductor structures formed on a same semiconductor substrate, wherein the first semiconductor structure comprises a first gate region, a first channel region, and first and second semiconductor regions, wherein the first gate region is on top of the first channel region and is oriented in a first direction, wherein the first channel region is sandwiched between the first and second semiconductor regions, wherein the second semiconductor structure comprises a second gate region, a second channel region, and third and fourth semiconductor regions, wherein the second gate region is on top of the second channel region and is oriented in a second direction, wherein the second channel region is sandwiched between the third and fourth semiconductor regions, wherein the first and second channel regions are of a same channel polarity, wherein the first and second directions are essentially parallel to a top surface of the semiconductor substrate and are not parallel to each other; and (b) a halo ion beam having a projected direction which is essentially a bisector direction of the first and second directions.

[Para 11] The present invention provides a novel method for forming the halo regions that minimizes the S/D doping reduction effect.

[Para 12] Brief Description of the Drawings

[Para 13] FIGs. 1A-1E show cross-sectional views of a semiconductor structure used to illustrate a first halo implant method, in accordance with embodiments of the present invention.

[Para 14] FIGs. 2A-2B show top views of another semiconductor structure used to illustrate a second halo implant method, in accordance with embodiments of the present invention.

[Para 15] FIGs. 3A-3D show top views of the semiconductor structure of FIGs. 2A-2B used to illustrate a third halo implant method, in accordance with embodiments of the present invention.

[Para 16] FIGs. 4A-4D show top views of the semiconductor structure of FIGs. 2A-2B used to illustrate a fourth halo implant method, in accordance with embodiments of the present invention.

[Para 17] Detailed Description of the Invention

[Para 18] FIGs. 1A-1E show cross-sectional views of a semiconductor structure 100 used to illustrate a first halo implant method, in accordance with embodiments of the present invention. More specifically, with reference to FIG.1A, in one embodiment, the fabrication process of the structure 100 starts out with the formation of a gate stack 120,130 (comprising a gate region 130 on a gate dielectric layer 120) on top of a semiconductor (silicon, germanium, etc.) substrate 110. The gate region 130 is electrically isolated from the substrate 110 by the gate dielectric layer 120.

[Para 19] Next, with reference to FIG.1B, in one embodiment, source/drain (S/D) extension regions 140a and 140b are formed in and at top surface of the substrate 110. In one embodiment, thin gate spacers (not shown) can be formed on side walls of the gate stack 120,130 by, illustratively, thermal oxidation before the formation of the S/D extension regions 140a and 140b. The S/D extension regions 140a and 140b can be lightly doped. Assume that the structure 100 is a transistor with an n-type channel. As a result, S/D extension regions 140a and 140b should be lightly doped with n-type dopants such as Arsenic atoms. In one embodiment, the S/D extension regions 140a and 140b can be formed by ion implantation with a low-energy ion beam of Arsenic ions.

[Para 20] In one embodiment, the S/D extension regions 140a and 140b extend under (i.e., undercut) the gate region 130. More specifically, the S/D extension regions 140a and 140b including undercutting portions 141a and 141b, respectively, can be formed in first and then second extension implanting steps. In the first extension implanting step, the dopant ion beam (used to form the S/D extension regions 140a and 140b) is directed at the structure 100 at a non-vertical direction represented by an arrow 142a (or in short, the direction 142a). As a result, the S/D extension regions 140a and 140b are formed, but only the S/D extension region 140a extends under the gate region 130 as the undercutting portion 141a. Next, in the second extension implanting step, the dopant ion beam is directed at the structure 100 at a non-vertical direction 142b. As a result, the S/D extension region 140b extends under the gate region 130 as the undercutting portion 141b.

[Para 21] Next, with reference to FIGs. 1C and 1D, in one embodiment of the first halo implant method, halo regions 150a and 150b are formed beneath the S/D extension regions 140a and 140b, respectively. The halo regions 150a and 150b can be doped with dopants of opposite type to the dopants of the S/D extension regions 140a and 140b. For example, if the substrate 110 is of p-type and the S/D extension regions 140a and 140b are doped with n-type dopants, the halo regions 150a and 150b can be doped with p-type dopants (such as Boron). In one embodiment, the halo regions 150a and 150b can be formed by ion implantation with a dopant ion beam of Boron ions.

[Para 22] In one embodiment, the halo regions 150a and 150b extend under (i.e., undercut) the gate region 130 (FIG. 1D). More specifically, the halo regions 150a and 150b including undercutting portions 151a and 151b, respectively, can be formed in first and second halo implanting steps. In the first halo implanting step, with reference to FIG. 1C, the dopant ion beam (used to form the halo regions 150a and 150b) is directed at the structure 100 at a non-vertical direction 152a. As a result, the halo regions 150a and 150b are formed, but only the halo region 150a extends under the gate region 130 as the undercutting portion 151a. In the second halo implanting step, with reference to FIG. 1D, the dopant ion beam is directed at the structure 100 at a

non-vertical direction 152b. As a result, the second halo region 150b extends under the gate region 130 as the undercutting portion 151b.

[Para 23] With reference back to FIG. 1C, in one embodiment, the direction 152a has a projected direction 152a' on a top surface 112 of the substrate 110, wherein the projected direction 152a' points from the S/D extension region 140a to the S/D extension region 140b and is essentially perpendicular to a direction of the gate region 130. The direction of the gate region 130 can be defined and represented by a vector (i.e., arrow) parallel to the interception line of the top surface 112 of the substrate 110 and a side wall 132 of the gate region 130. In FIG. 1C, the interception line (not shown) is perpendicular to the cross-sectional plane depicted in FIG. 1C. The direction of the gate region 130 can point into or point out of the cross-sectional plane depicted in FIG. 1C.

[Para 24] Similarly, with reference to FIG. 1D, in one embodiment, the direction 152b has a projected direction 152b' on the top surface 112 of the substrate 110, wherein the projected direction 152b' points from the S/D extension region 140b to the S/D extension region 140a and is essentially perpendicular to the direction of the gate region 130.

[Para 25] Next, with reference to FIG. 1E, in one embodiment, gate spacers 170a and 170b can be formed on side walls of the gate stack 130,120. In one embodiment, the gate spacers 170a and 170b comprise a nitride (e.g., silicon nitride). Next, the gate stack 130,120 and the gate spacers 170a and 170b are used as a mask for doping source/drain (S/D) regions 160a and 160b in and at top surface of the substrate 110. In one embodiment, the S/D region 160a can overlap with the S/D extension region 140a and the halo region 150a. Similarly, the S/D region 160b can overlap with the S/D extension region 140b and the halo region 150b.

[Para 26] The S/D regions 160a and 160b can be heavily doped with dopants of the same type as that of the S/D extension regions 140a and 140b. For example, if the S/D extension regions 140a and 140b are doped with n-type dopants, the S/D regions 160a and 160b can be heavily doped with n-type

dopants (such as phosphorous). In one embodiment, the S/D regions 160a and 160b can be formed by ion implantation using a high-energy ion beam of dopants.

[Para 27] In one embodiment, multiple structures (not shown) similar to the structure 100 can be formed on a same wafer. Assume that the directions of the gate regions of these structures are parallel to each other (i.e., these structures have only one gate orientation). As a result, the first and second extension implanting steps and then the first and second halo implanting steps) can be performed only once (as described above) for all of these structures. Assume otherwise that these structures have two different gate orientations with some of the structures having a first gate orientation and the others having a second gate orientation. As a result, the first and second extension implanting steps and then the first and second halo implanting steps can be performed first for the structures having the first gate orientation. Then, the first and second extension implanting steps and then the first and second halo implanting steps can be performed one more time for the structures having the second gate orientation.

[Para 28] FIGs. 2A-2B show top views of a semiconductor structure 200 used to illustrate a second halo implant method, in accordance with embodiments of the present invention. The structure 200 comprises, illustratively, transistors 201 and 202 fabricated on a same semiconductor substrate 210. The transistor 201 comprises, illustratively, a gate region 231 formed on top of a channel region (not shown) which is sandwiched between two S/D regions 261a and 261b. Similarly, the transistor 202 comprises, illustratively, a gate region 232 formed on top of a channel region (not shown) which is sandwiched between two S/D regions 262a and 262b. In one embodiment, the transistors 201 and 202 are of a same channel polarity (e.g., n-type channel).

[Para 29] In one embodiment, the formation of each transistor of the transistors 201 and 202 (FIG. 2A) is similar to the formation of the structure 100 (FIG. 1E), except for the formation of the halo regions (not shown). In one

embodiment, the second halo implant method comprises first and second halo ion bombardments (i.e., halo ion beams).

[Para 30] In one embodiment, with reference to FIG. 2A, the first halo ion bombardment of the second halo implant method has a projected direction 251 (i.e., the first halo ion bombardment of the second halo implant method has a direction whose projected direction on the top surface 212 of the substrate 210 is the projected direction 251). In one embodiment, the projected direction 251 is essentially a bisector direction of a direction 281 of the gate region 231 and a direction 282 of the gate region 232.

[Para 31] Next, with reference to FIG. 2B, the second halo ion bombardment of the second halo implant method has a projected direction 252 which is essentially opposite to the projected direction 251 (FIG. 2A). For instance, if the projected direction 251 (FIG. 2A) is Northwest-Southeast, the projected direction 252 can be Southeast-Northwest as shown. As a result, after the first and second halo ion bombardments of the second halo implant method, all the resulting halo regions (not shown) of both transistors 201 and 202 have the desired undercutting portions under the respective gate regions 231 and 232.

[Para 32] In one embodiment, the directions 281 and 282 are perpendicular to each other. Assume that the direction 281 is North-South and the direction 282 is West-East. As a result, the projected direction 251 (FIG. 2A), as a bisector direction of the directions 281 and 282, can be essentially Northwest-Southeast, whereas the projected direction 252 (FIG. 2B) can be essentially Southeast- Northwest as shown.

[Para 33] FIGs. 3A-3D show top views of the semiconductor structure 200 of FIGs. 2A-2B used to illustrate a third halo implant method, in accordance with embodiments of the present invention. More specifically, in one embodiment, the third halo implant method comprises four (first, second, third, and fourth) halo ion bombardments.

[Para 34] In one embodiment, with reference to FIG. 3A, the first halo ion bombardment of the third halo implant method has a projected direction 351 which is essentially perpendicular to the direction 281 of the gate region 231 and going from the S/D region 261a towards the gate region 231. In one embodiment, the first halo ion bombardment of the third halo implant method is performed while the transistor 202 is covered by a first mask (not shown) so that the transistor 202 is not affected by the first halo ion bombardment of the third halo implant method.

[Para 35] Next, in one embodiment, with reference to FIG. 3B, the second halo ion bombardment of the third halo implant method has a projected direction 352 which is essentially perpendicular to the direction 281 of the gate region 231 and going from the S/D region 261b towards the gate region 231. In one embodiment, the first halo ion bombardment of the third halo implant method is performed while the transistor 202 is still covered by the first mask.

[Para 36] Next, in one embodiment, with reference to FIG. 3C, the third halo ion bombardment of the third halo implant method has a projected direction 353 which is essentially perpendicular to the direction 282 of the gate region 232 and going from the S/D region 262a towards the gate region 232. In one embodiment, the third halo ion bombardment of the third halo implant method is performed while the transistor 201 is covered by a second mask (not shown) so that the transistor 201 is not affected by the third halo ion bombardment of the third halo implant method (in one embodiment, the first mask is removed before the second mask is put in place).

[Para 37] Next, in one embodiment, with reference to FIG. 3D, the fourth halo ion bombardment of the third halo implant method has a projected direction 354 which is essentially perpendicular to the direction 282 of the gate region 232 and going from the S/D region 262b towards the gate region 232. In one embodiment, the fourth halo ion bombardment of the third halo implant method is performed while the transistor 201 is still covered by the second mask.

[Para 38] In one embodiment, the directions 281 and 282 in FIG. 3A-3D are perpendicular to each other. Assume that the direction 281 is North-South and the direction 282 is West-East. As a result, the projected directions 351 (FIG. 3A), 352 (FIG. 3B), 353 (FIG. 3C), 354 (FIG. 3D) can be essentially West-East, East-West, North-South, and South-North, respectively.

[Para 39] FIGs. 4A-4D show top views of the semiconductor structure 200 of FIGs. 2A-2B used to illustrate a fourth halo implant method, in accordance with embodiments of the present invention. More specifically, in one embodiment, the fourth halo implant method comprises four (first, second, third, and fourth) halo ion bombardments.

[Para 40] In one embodiment, with reference to FIG. 4A, the first halo ion bombardment of the fourth halo implant method has a projected direction 451 which is essentially perpendicular to the direction 281 of the gate region 231 and going from the S/D region 261a towards the gate region 231. In one embodiment, the first halo ion bombardment of the fourth halo implant method is performed while the transistor 202 and essentially a half of the transistor 201 corresponding to the side of the S/D region 261b are covered by a third mask (not shown) so that the transistor 202 and the half of the transistor 201 corresponding to the side of the S/D region 261b are not affected by the first halo ion bombardment of the fourth halo implant method.

[Para 41] Next, in one embodiment, with reference to FIG. 4B, the second halo ion bombardment of the fourth halo implant method has a projected direction 452 which is essentially perpendicular to the direction 281 of the gate region 231 and going from the S/D region 261b towards the gate region 231. In one embodiment, the first halo ion bombardment of the fourth halo implant method is performed while the transistor 202 and essentially a half of the transistor 201 corresponding to the side of the S/D region 261a are covered by a fourth mask (not shown) so that the transistor 202 and the half of the transistor 201 corresponding to the side of the S/D region 261a are not affected by the second halo ion bombardment of the fourth halo implant

method (in one embodiment, the third mask is removed before the fourth mask is put in place).

[Para 42] Next, in one embodiment, with reference to FIG. 4C, the third halo ion bombardment of the fourth halo implant method has a projected direction 453 which is essentially perpendicular to the direction 282 of the gate region 232 and going from the S/D region 262a towards the gate region 232. In one embodiment, the third halo ion bombardment of the fourth halo implant method is performed while the transistor 201 and essentially a half of the transistor 202 corresponding to the side of the S/D region 262b are covered by a fifth mask (not shown) so that the transistor 201 and the half of the transistor 202 corresponding to the side of the S/D region 262b are not affected by the third halo ion bombardment of the fourth halo implant method (in one embodiment, the fourth mask is removed before the fifth mask is put in place).

[Para 43] Next, in one embodiment, with reference to FIG. 4D, the fourth halo ion bombardment of the fourth halo implant method has a projected direction 454 which is essentially perpendicular to the direction 282 of the gate region 232 and going from the S/D region 262b towards the gate region 232. In one embodiment, the fourth halo ion bombardment of the fourth halo implant method is performed while the transistor 201 and essentially a half of the transistor 202 corresponding to the side of the S/D region 262a are covered by a sixth mask (not shown) so that the transistor 201 and the half of the transistor 202 corresponding to the side of the S/D region 262a are not affected by the fourth halo ion bombardment of the fourth halo implant method (in one embodiment, the fifth mask is removed before the sixth mask is put in place).

[Para 44] In one embodiment, the directions 281 and 282 in FIG. 4A-4D are perpendicular to each other. Assume that the direction 281 is North-South and the direction 282 is West-East. As a result, the projected directions 451 (FIG. 4A), 452 (FIG. 4B), 453 (FIG. 4C), 454 (FIG. 4D) can be essentially West-East, East-West, North-South, and South-North, respectively, as shown.

[Para 45] With reference back to FIG. 4A, the third mask is shown to cover the entire transistor 202, the entire S/D region 261b, and a right portion of the gate region 231. Alternatively, due to mask fabrication tolerance, the third mask can cover the entire transistor 202 and a right portion of the S/D region 261b, leaving the entire S/D region 261a, the entire gate region 231, and a left potion of the S/D region 261b exposed to halo bombardment. In This case may be acceptable, but the width of the exposed left portion of the S/D region 261b (measured in a direction perpendicular to the direction of the gate region 231) should be kept as small as possible to minimize unwanted halo implants in the S/D region 261b as a result of the halo bombardment in the projected direction 451. The optimum case is shown in FIG. 4A where the third mask covers the entire S/D region 261b. Similar considerations are applicable to the fourth, fifth, and sixth masks.

[Para 46] In summary, in each of the second and third halo implant methods of the present invention (described *supra* with reference to FIGs. 2A-2D, and 3A-3D), each of the S/D regions 261a, 261b, 262a, and 262b is subjected to only two halo ion bombardments. Especially, in the fourth halo implant method of the present invention (described *supra* with reference to FIGs. 4A-4D), each of the S/D regions 261a, 261b, 262a, and 262b is subjected to only one halo ion bombardments.

[Para 47] In the embodiments described above with reference to FIGs. 2 and 3, the structure 200 have two transistors 201 and 202 having two respective gate orientations. Alternatively, the structure 200 can have two or more transistors similar to the transistors 201 and 202 but having only one gate orientation. As a result, the number of masks and halo implanting steps can be reduced.

[Para 48] More specifically, with reference to FIGs. 3A-3D, assume that the two transistors 201 and 202 have the same gate orientation (e.g., both the gate regions 231 and 232 run in the North-South direction). As a result, the first and second masks are not needed for the third halo implant method. Also, only the first and second halo ion bombardments in the projected

directions 351 and 352, respectively, are needed (the third and fourth halo ion bombardments in the projected directions 353 and 354 are not needed).

[Para 49] With reference to FIGs. 4A-4D, assume that the two transistors 201 and 202 have the same gate orientation (e.g., both the gate regions 231 and 232 run in the North-South direction). As a result, only two masks (seventh and eighth) masks are needed, as opposed to four masks (third, fourth, fifth, and sixth masks) needed in the above embodiments. The seventh mask can cover the two right S/D regions of the transistors 201 and 202 while the two left S/D regions of the transistors 201 and 202 are subjected to the halo ion bombardment in projected direction 451 (FIG. 4A). Then, the seventh mask can be removed and the eighth mask can cover the two left S/D regions of the transistors 201 and 202 while the two right S/D regions of the transistors 201 and 202 are subjected to the halo ion bombardment in projected direction 452 (FIG. 4B). In total, only two halo ion bombardments in the projected directions 452 and 453 (FIGs. 4A and 4B, respectively) are needed instead of four as described above with reference to FIGs. 4A-4D.

[Para 50] While particular embodiments of the present invention have been described herein for purposes of illustration, many modifications and changes will become apparent to those skilled in the art. Accordingly, the appended claims are intended to encompass all such modifications and changes as fall within the true spirit and scope of this invention.